ECE 222 Final Project Report

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1. Introduction

This project aims to build a practical single-stage headphone amplifier using the CMOY architecture to amplify common audio signals for use with devices like Apple EarBuds. Our team selected a non-inverting amplifier configuration using the OPA1656 op-amp, along with dual BUF634A buffer stages for better current drive. The CMOY amplifier, originally designed by Chu Moy, is known for its compact layout, clean audio performance, and accessibility for beginners. Our main tasks included drafting the amplifier schematic based on the CMOY design, verifying functionality through simulation, assembling the circuit on a Printed Circuit Board (PCB), and testing the final build with an oscilloscope.

2. Schematic

The schematic was created based on the standard CMOY layout provided.

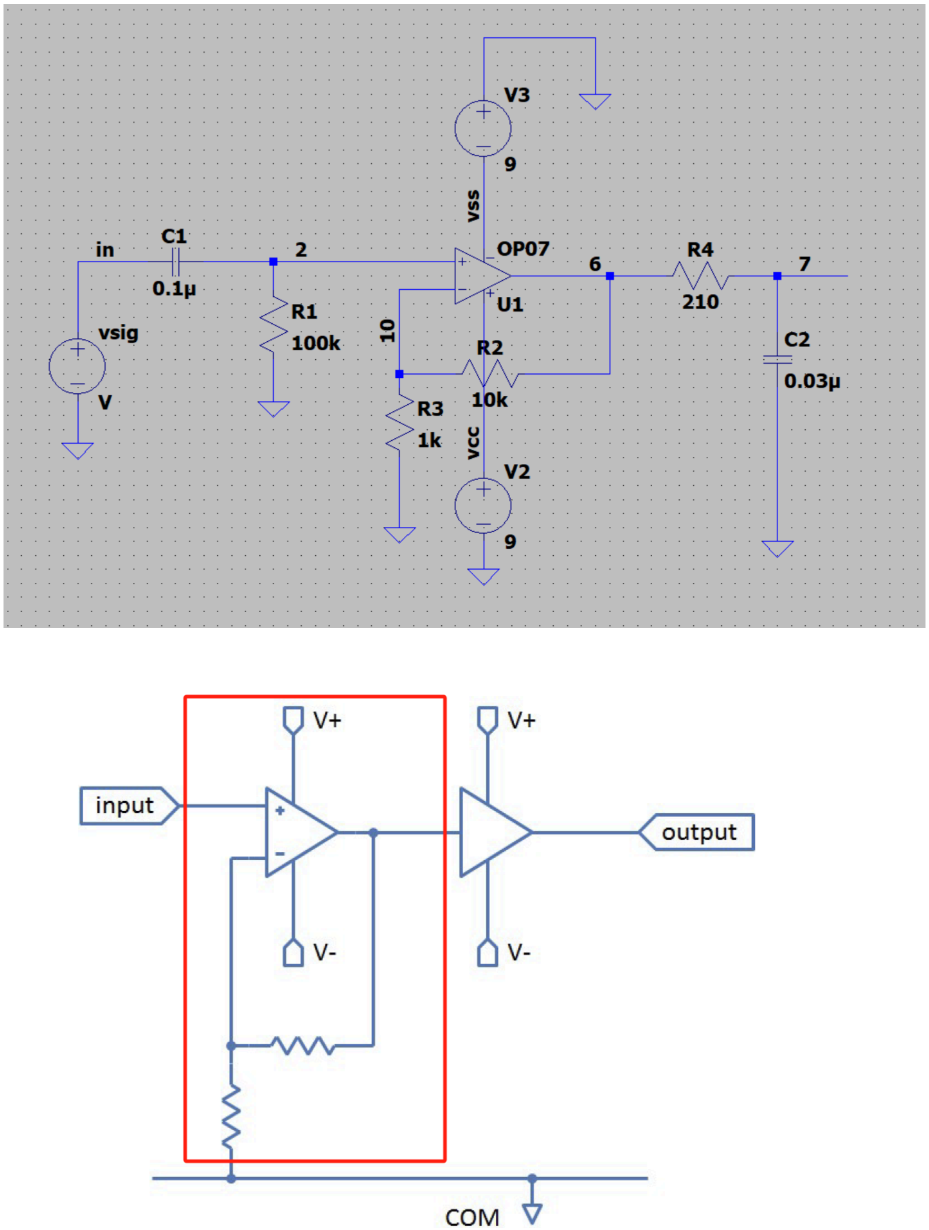

Figure 1: Amplifier Schematic with Buffer Setup

3. Design Requirements

- Output Load Impedance: RL = 32 Ω (nominal), up to 300 Ω (max).
- Maximum Output Power (RMS): Pout, RMS ≥ 100 mW/ch with RL = 32 Ω.
- Amplifier Output Impedance: Rout < 5 Ω.

• Amplifier Input Impedance: $R_{in} \geq 10$ kΩ.

• Audio Input Signal Amplitude: $V_{in,RMS} = 0.3$ V (nominal), $V_{in,max} = 1$ V (peak-to-peak).

• Audio Input Source Impedance: $R_{sig} = 100$ Ω.

• 3-dB Small-Signal Bandwidth: 18 Hz − 25 kHz (nominal).

• Full-Power Bandwidth: > 20 kHz.

• Total Harmonic Distortion: THD < 0.1% or −60 dB at 1 kHz with $P_{out,RMS} = 100$ mW and $R_L = 32$ Ω.

• Power Supply Options: Dual rail = ±12 V (regulated power supply)

• Power Consumption: $I_{dd,avg} \approx I_{ss,avg} < 50$ mA; $I_{dd,peak} \approx I_{ss,peak} < 100$ mA; $PD = |V_{dd} \cdot I_{dd}| + |V_{ss} \cdot I_{ss}|$

4. Circuit Design

The gain is set using resistors R2 and R3 in the feedback path:

- $A_v = 1 + (R2 / R3) = 11$

Resistor and capacitor values were selected based on calculated needs for gain, cutoff frequency, and impedance. Our team used the following components:

- R1: 100kΩ – Sets input bias
- R2: 10kΩ, R3: 1kΩ – Gain-setting
- R4: 210Ω – Output stability
- C1: 1μF – Input coupling
- C2: 0.03μF – Output decoupling

OPA1656 was chosen for its high slew rate and low distortion. BUF634A was used for buffering high current loads.

```
$DATA1 SOURCE='PrimeSim HSPICE' VERSION='T-2022.06-SP1-2 win64' PARAM_COUNT=0
.TITLE '**** ece 222 course project ****'
 gain_mid          gain_db           bw_f1             bw_f2
 bw_3db            temper            alter#
    9.7972           19.8221            1.5946           2.514e+04
  2.514e+04          27.0000          1
```

Figure 2: Simulation result of large-signal gain vs. frequency (full-power bandwidth)

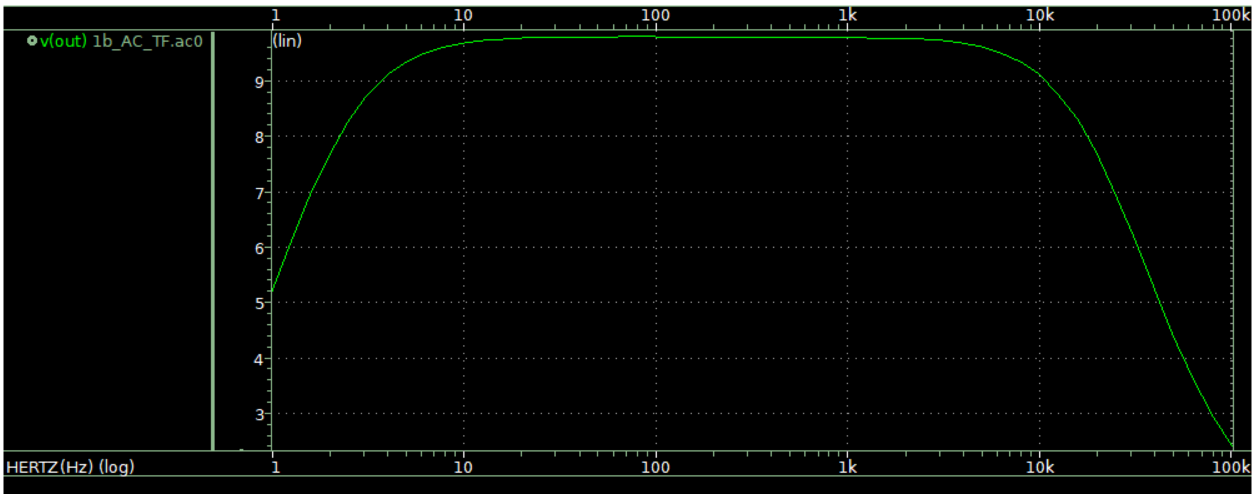

Figure 3: Mid-band small-signal gain vs. frequency

5. Simulation

```
$DATA1 SOURCE='PrimeSim HSPICE' VERSION='T-2022.06-SP1-2 win64' PARAM_COUNT=0
.TITLE '**** ece 222 course project ****'
 zin_1k            zin_5k            zin_10k           zin_15k
 zin_20k           temper            alter#
  1.000e+05         1.000e+05         1.000e+05         1.000e+05
  1.000e+05          27.0000          1
```

Figure 4: Input impedance magnitude vs. frequency

```
$DATA1 SOURCE='PrimeSim HSPICE' VERSION='T-2022.06-SP1-2 win64' PARAM_COUNT=0
.TITLE '**** ece 222 course project ****'
 zout_1k          zout_5k          zout_10k         zout_15k
 zout_20k         temper           alter#
    3.9288           3.9343           3.9353           3.9353
    3.9357          27.0000          1
```

Figure 5: Output impedance magnitude vs. frequency

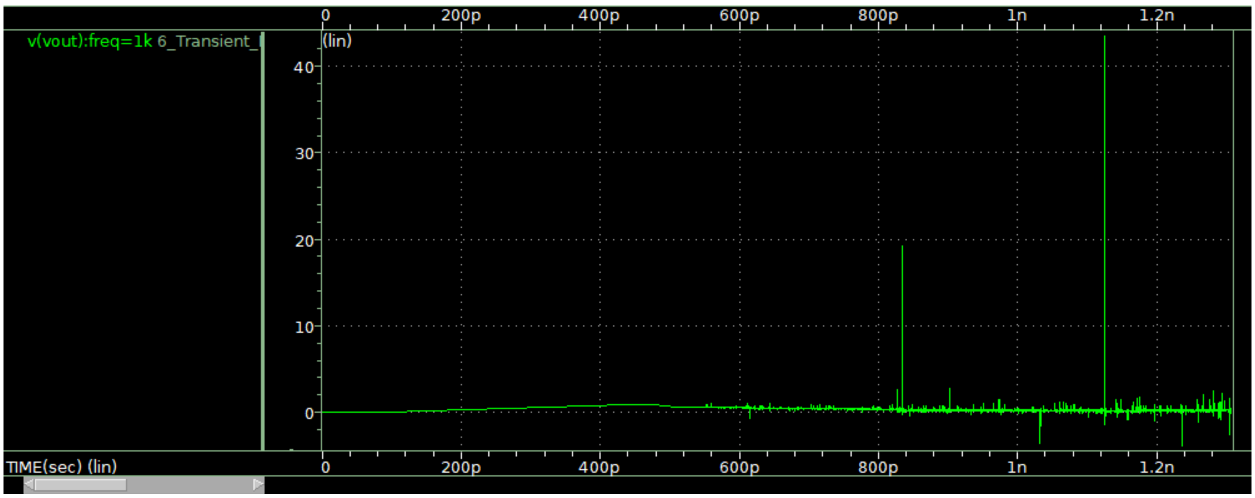

Figure 6: Measured slew-rate vs. frequency (slew-rate limit characterization)

```
$DATA1 SOURCE='PrimeSim HSPICE' VERSION='T-2022.06-SP1-2 win64' PARAM_COUNT=0
.TITLE '**** ece 222 course project ****'
 vout_peak        vout_pp          pout_rms         idd_avg
 iss_avg          idd_peak         iss_peak         temper
 alter#
    4.2708           8.2116           0.2634          -4.842e-02
  4.328e-02         -0.1384           0.1281          27.0000
1
```

Figure 7: Transient large-signal output waveform at a representative frequency

```
$DATA1 SOURCE='PrimeSim HSPICE' VERSION='T-2022.06-SP1-2 win64' PARAM_COUNT=0
.TITLE '**** ece 222 course project ****'
 thd_db           sndr_db          temper           alter#
 -105.8391           4.3843          27.0000          1
```

Figure 8: Measured TUD for the output step response

6. Amplifier PCB

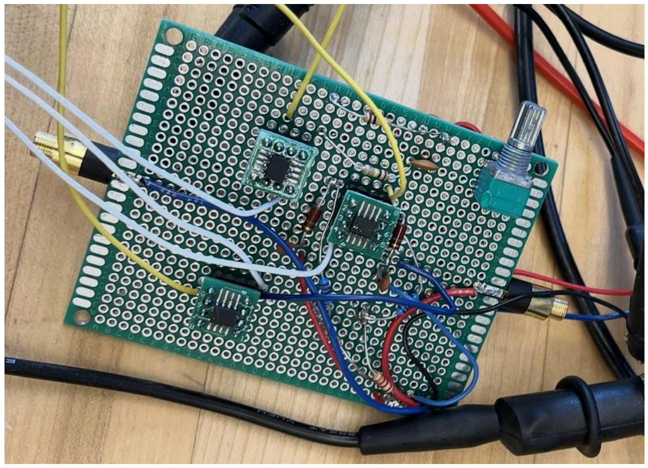

Figure 9: PCB implementation of the headphone amplifier

Figure 10: Amplifier output signals

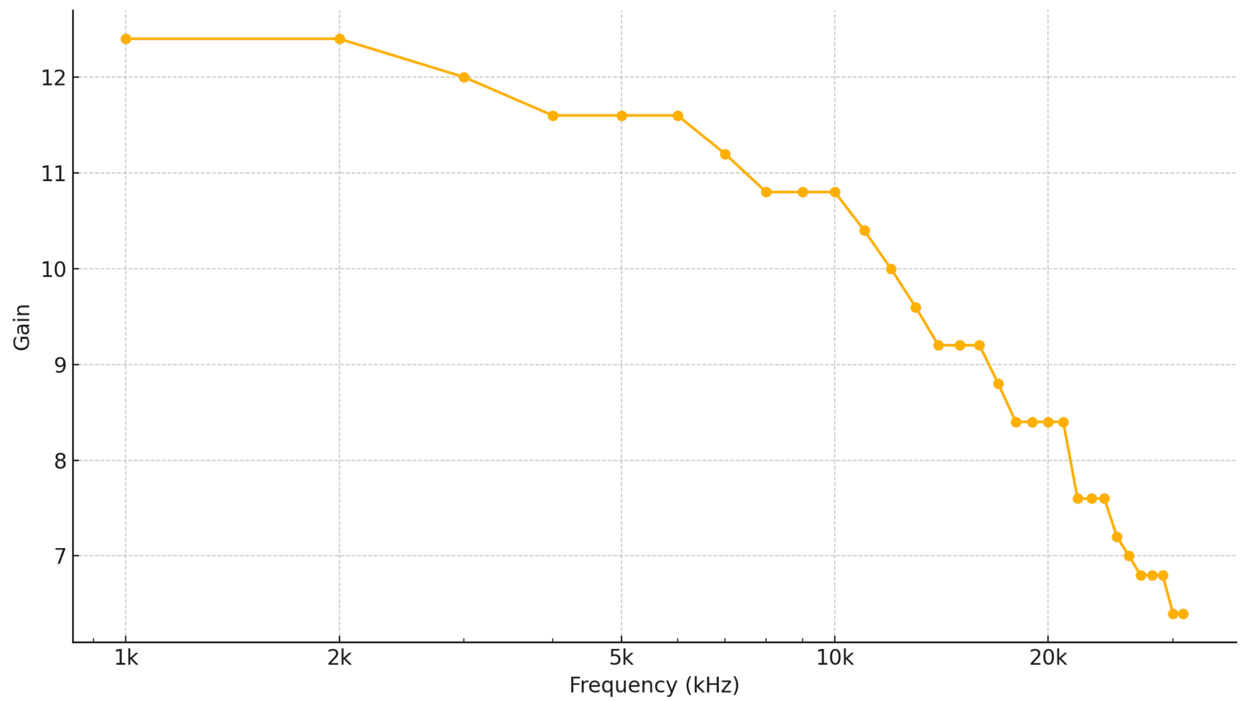

Figure 11: Gain vs. frequency

7. Measurements

For the bandwidth test, our team gradually increased the input frequency from 1 kHz up to 100 kHz and tracked how the gain changed. The −3 dB points on either side of the mid-band gain were used to estimate the bandwidth range.

To check the input impedance, our team inserted a 1kΩ resistor between the signal source and the amplifier, using a 0.3 V input. Measuring the voltage drop across the resistor allowed us to find the current flowing into the circuit. With that and the input voltage reading, we estimated the input impedance using the ratio of voltage to current.

All measurements:

- Input: 10kHz sinusoid, 1.0Vpp
- Left channel gain: ~9.38

- Right channel gain: ~8.43
- Bandwidth: ~20 kHz
- Input impedance: ~6kΩ
- Output impedance: ~4Ω

8. Conclusion

Overall, this project provided valuable hands-on experience in applying analog amplification concepts from class. The tasks ranged from selecting an appropriate architecture to fine-tuning the design for practical use. The final amplifier performed as intended and delivered amplified audio with stable output power. In the future, we would consider improving the input stage for better impedance matching and using a dual-channel potentiometer to achieve more balanced volume control. Additional features like tone adjustment or power-saving modes could also be worth exploring.